Application No. 10/771,023

MXIC 1564-1
(P920205US)

Amendment NOT Entered 6/8/06 C/M

DO NOT ENTER

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (previously presented) An integrated circuit, comprising:

an array of memory cells, the array configured as a NAND array in a plurality of columns and rows of memory cells, the columns comprising one or more sets of memory cells in series coupled to a bit line, and the rows comprising sets of memory cells having their respective gate terminals coupled to a word line, memory cells in the array respectively comprising a gate terminal, a first channel terminal, a second channel terminal and a channel region between the first and second channel terminals, a charge trapping structure over the channel region, a tunneling dielectric between the channel region and the charge trapping structure, and a blocking dielectric between the charge trapping structure and the gate terminal;

circuitry to program the memory cells in the array by E-field assisted tunneling through the tunneling dielectric by applying a positive voltage to the gate terminal and a low voltage or ground to the first and second channel terminals, while limiting program and erase cycling; and

circuitry to read data from the memory cells.

2. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a barrier height and thickness sufficient to prevent direct tunneling.

3. (original) The integrated circuit of claim 1, wherein the tunneling dielectric has a silicon-dioxide equivalent thickness between about 30 Angstroms and about 70 Angstroms.

4. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness greater than 30 Angstroms.

5. (original) The integrated circuit of claim 1, wherein the tunneling dielectric comprises silicon dioxide, and has a thickness between about 30 Angstroms and about 70 Angstroms.

6. (original) The integrated circuit of claim 1, wherein the positive voltage is about 15 Volts or greater.